Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electronic device, comprising:

a controller programmed to produce first address data on an output thereof;

a plurality of integrated circuits (ICs) addressable by the controller; and

a shared bus, said shared bus joining the controller and the plurality of ICs such that the controller is able to send data to the plurality of ICs over the shared bus;

wherein each IC of the plurality of ICs comprises:

an input for receiving address data, said address data representing an address of the IC on the shared bus~~, and an~~;

an address register for storing the received address data as the address of the IC on the shared bus;

output generator logic for ~~providing~~ modifying the received address data to produce modified address data that is different from the received address data, said modified address data representing an address of another IC on the shared bus; and

an output for providing the modified address data;

wherein the input of a first IC of the plurality of ICs communicates with the output of the controller, and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration~~.~~;

wherein the first address data produced on the output of the controller represents an address of the first IC on the shared bus; and

wherein the modified address data provided on the output of each IC of the plurality of ICs represents an address of a corresponding succeeding IC in the daisy chain configuration on the shared bus.

2. – 4. (Cancelled)

5. (Original) The electronic device claimed in claim 1, wherein the address data comprises a binary word.

6. (Original) The electronic device claimed in claim 1, wherein the address data comprises a series of pulses representing an address value.

7. (Currently Amended) The electronic device claimed in claim 1, further comprising a storage medium in communication with the controller and having stored therein programming instructions for instructing the controller to produce the first address data on the output thereof.

8. (Currently Amended) An electronic device, comprising:

means for generating first address data at an output of a controller;

means for receiving the first address data at an input of a first integrated circuit (IC);

means for storing the first address data in the first IC as an address of the first IC;

means for modifying the first address data in the first IC to produce first modified address data different from the first address data; and

means for providing the first modified address data to a second IC through an output of the first IC, said first modified address data representing an address of the second IC.

9. (Currently Amended) A method for initializing addresses of a plurality of integrated circuits (ICs), comprising:

generating first address data at an output of a controller;

receiving the first address data at an input of a first IC;

storing the first address data in an address register of the first IC as an address of the first IC;

modifying the first address data in the first IC to produce first modified address data different from the first address data; and

providing the first modified address data to a second IC through an output of the first IC, said first modified address data representing an address of the second IC.

10. (Currently Amended) The method for initializing claimed in claim 9, further comprising:

receiving the first modified address data at an input of a second IC;

storing the first modified address data in an address register of the second IC, as the address of the second IC;

modifying the first modified address data in the second IC to produce second modified address data; and

providing the second modified address data ~~at~~ to a third IC through an output of the second IC, said second modified address data representing an address of the third IC.

11. (Currently Amended) An electronic device, comprising:

a controller;

a plurality of integrated circuits (ICs) addressable by the controller; and

a shared bus joining the controller and the plurality of integrated circuits;

wherein the controller is programmed to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses,

wherein each IC of the plurality of ICs comprises:

an input for receiving an input enable signal ~~and~~;

an output for providing an output enable signal to another IC in conjunction with a change in address data on the shared bus~~, and~~;

a shared bus input for receiving addresses present on the shared bus; and

means for storing an address present on the shared bus as an address of the IC in response to receiving ~~an~~ the input enable signal~~, and~~;

wherein the input of a first IC of the plurality of ICs communicates with the output of the controller, and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration~~.~~;

wherein the first address of the series of addresses produced by the controller on the shared bus represents an address of the first IC on the shared bus, and each succeeding address of the series of addresses produced by the controller on the shared bus represents an address of a corresponding succeeding IC in the daisy chain configuration; and

wherein the enable signal produced on the output of the controller is received at the input of the first IC as the input enable signal for the first IC, and the output enable signal provided on the output of each IC of the plurality of ICs is received at the input of a corresponding succeeding IC in the daisy chain configuration as the input enable signal for the corresponding succeeding IC.

12. (Currently Amended) The electronic device claimed in claim 11, wherein each IC of said plurality of ICs further comprises a first logic circuit for storing ~~an~~ the address present on the shared bus as ~~an~~ the address of the IC upon receipt of ~~an~~ the input enable signal.

13. (Currently Amended) The electronic device claimed in claim 12, wherein each IC of said plurality of ICs further comprises a second logic circuit for generating ~~an~~ the output enable signal in conjunction with ~~a~~ the change in address data on the shared bus.

14. (Currently Amended) The electronic device claimed in claim 13, wherein said second logic circuit of each IC of the plurality of ICs comprises a timer that is initialized upon receipt of ~~an~~ the input enable signal, and that generates ~~an~~ the output enable signal after a period of time that coincides with a rate of change of address data on the shared bus.

15. (Currently Amended) The electronic device claimed in claim 13, wherein said second logic circuit of each IC of the plurality of ICs produces ~~an~~ the output enable signal upon detecting a first change in address data on the shared bus after receiving ~~an~~ the input enable signal.

16. (Currently Amended) The electronic device claimed in claim 11, wherein each IC of said plurality of ICs comprises a processor programmed to initialize a timer upon receipt of ~~an~~ the input enable signal, and to generate ~~an~~ the output enable signal upon expiration of the timer.

17. (Currently Amended) The electronic device claimed in claim 11, wherein each IC of said plurality of ICs comprises a processor programmed to receive ~~an~~ the input enable signal at the input, store the address data present on the shared bus as the address of the IC in response to the input enable signal, detect ~~a~~ the change in the address data on the shared bus, and generate ~~an~~ the output enable signal at the output in response to the change in the address data.

18. (Currently Amended) The electronic device claimed in claim 11, wherein each IC of said plurality of ICs comprises:

means for receiving ~~an~~ the input enable signal at the input; and

means for generating ~~an~~ the output enable signal at the output in conjunction with the change in the address data.

19. (Currently Amended) The electronic device claimed in claim 11, further comprising a storage medium in communication with the controller and having stored therein programming instructions for instructing the controller to produce ~~a~~ the series of addresses on the shared bus and to produce ~~an~~ the enable signal on ~~an~~ the output in conjunction with ~~a~~ the first address of the series of addresses.

20. (Currently Amended) An electronic device, comprising:

means for generating an enable signal at an output of a controller and generating first address data on a shared bus;

means for receiving the enable signal generated at the output of the controller at an input of a first integrated circuit (IC);

means for receiving the first address data at a shared bus input of the first IC;

means for storing the first address data in an address register of the first IC as an address of the first IC upon coincidence of receiving the enable signal and receiving the first address data; and

means for providing an output enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus.

21. (Currently Amended) A method for initializing addresses of a plurality of integrated circuits (ICs), comprising:

generating an enable signal at an output of a controller and generating first address data on a shared bus;

receiving the enable signal generated at the output of the controller at an input of a first IC;

receiving the first address data at a shared bus input of the first IC;

storing the first address data in an address register of the first IC as an address of the first IC upon coincidence of receiving the enable signal and receiving the first address data; and

providing ~~an~~ a first output enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus.

22. (Currently Amended) A method as claimed in claim 21, further comprising:

generating second address data on the shared bus;

receiving the first output enable signal provided at the output of the first IC at the input of a second IC;

receiving the second address data at a shared bus input of the second IC;

storing ~~a~~ the second address data present on the shared bus in an address register of the second IC as an address of the second IC upon coincidence of receiving the first output enable signal and receiving the second address data; and

~~generating an~~providing a second output enable signal at an output of the second IC to an input of a third IC in conjunction with a change in address data present on the shared bus.

23. (Currently Amended) The method claimed in claim 21, wherein ~~generating~~ providing the first output enable signal at the output of the first IC comprises:

initializing a timer upon receipt of the enable signal at the input of the first IC, and generating the first output enable signal at the output of the first IC upon expiration of the timer.

24. (Currently Amended) The method claimed in claim 21, wherein the first output enable signal is generated at the output of the first IC upon detection of a change in address data after receiving ~~an~~ the enable signal at the input of the first IC.

25. (Previously Presented) The electronic device claimed in claim 1, wherein the modified address data is incremented address data.

26. (Cancelled)

27. (Currently Amended) The electronic device claimed in claim ~~3~~ 1, wherein the output generator logic modifies the address data by incrementing the address data.

28. (Cancelled)

29. (Previously Presented) The electronic device claimed in claim 8, wherein the means for modifying the first address data comprises a means for incrementing the first address data.

30. (Previously Presented) The method of claim 9, wherein the step of modifying the first address data in the first IC to produce first modified address data different from the first address data, comprises:

incrementing the first address data in the first IC to produce first modified address data different from the first address data.

31. (Previously Presented) The method of claim 10, wherein the step of modifying the first modified address data in the second IC to produce second modified address data, comprises:

incrementing the first modified address data in the second IC to produce second modified address data.

32. (Previously Presented) The electronic device of claim 11, wherein each address of the series of addresses produced by the controller on the shared bus is different.

33. (New) The electronic device of claim 1,

wherein, after the first IC has stored the first address data in the address register of the first IC as the address of the first IC on the shared bus, the controller is configured to cause the first IC to execute an operation by sending a command to execute the operation over the shared bus, said command including the address of the first IC.

34. (New) The electronic device of claim 11,

wherein, after the first IC has stored the first address data in said means for storing an address of the first IC as the address of the first IC on the shared bus, the controller is configured to cause the first IC to execute an operation by sending a command to execute the operation over the shared bus, said command including the address of the first IC.